## REMARKS

Favorable reconsideration of this application, in light of the preceding amendments and following remarks, is respectfully requested.

Claims 1-8 are pending in this application, and claim 1 is independent.

Applicant has filed an Information Disclosure Statement (IDS) on December 22, 2008. The Examiner is respectfully requested to consider the references cited in the IDS and indicate the same in the next Office communication.

## CLAIM OBJECTIONS

Claims 1 is objected to because of the following informalities: In line 22, "correct" should be replaced with --current--.

As shown in the preceding section, Applicant has amended claim 1 as suggested by the Examiner. Reconsideration and allowance of claim 1 is respectfully requested.

## REJECTIONS UNDER 35 U.S.C. § 103

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al. ("On the Power Dissipation in Dynamic Threshold Silicon-on-Insulator CMOS Inverter," IEEE Transactions on Electron Devices, Vol. 45, No. 8, August 1998, hereinafter "Jin") in view of Ishibashi et al. (USP 6,864,539, hereafter "Ishibashi") and further in view of Shimomura et al. (JP 10-189957, hereafter "Shimomura"). This rejection is respectfully traversed.

Claim 1 recites a lateral bipolar CMOS integrated circuit wherein, among other things, a forward pulse current flows from the current source connected with the p-type base terminal of the n-channel MOS transistor to the p-type base terminal **in synchronization to switching when the input voltage to the gate input terminal switches from the low level to the high level**. (Emphasis Added)

The Examiner admits that Jin fails to teach each and every limitation of claim 1 and relies on the teachings of Ishibashi and Shimomura to cure the noted deficiencies of Jin.

The Examiner alleges that the recitation "current source connected with the p-type base terminal of the n-channel MOS transistor" of claim 1 reads on the current source 4 in FIGS. 6 and 7 of Ishibashi and the recitation "p-type base terminal" of claim 1 reads on the p-well 20 (Vbn) in FIGS. 6 and 7 of Ishibashi. The Examiner further alleges that column 9, lines 51-67 to column 6, lines 1-8 of Ishibashi teach supplying "a forward pulse current" from current source 4 to p-well 20 (Vbn) as required by claim 1.

The sections of Ishibashi pointed out by the Examiner describe the circuit diagram of FIG. 7. FIG. 7 of Ishibashi illustrates a configuration of the semiconductor device of FIG. 6 including current source 4. Ishibashi states that when the control signal Cbn is at the high level "H", the current Ibn flows from the high potential power supply line (Vdd) to the low potential power supply line (Vss) via the pMOS transistor 44, the p-well 20 (Vbn), and the diode 21. Ishibashi provides absolutely no indication that this flow of current is "**in synchronization to switching when the input voltage to the gate input terminal switches from the low level to the high level**," as required by claim 1. (Emphasis Added)

The Examiner also relies on the teaching of Shimomura in paragraph [**0016**] to teach the above mentioned limitation of claim 1.

However, in paragraph [**0016**], Shimomura, <u>at most</u>, teaches applying a back potential to a transistor. For example, as illustrated in FIG. 2, Shimomura teaches applying back potential BP generated by the bias control circuit 103 to transistor 101 and a back potential BN generated by the bias control circuit 104 to the transistor 102. Shimomura fails to disclose "a forward pulse current flows from the current source connected with the p-type base terminal of the n-channel MOS

transistor to the p-type base terminal," as recited in claim 1, let alone a forward current pulse in synchronization with the input.

Absent any such teachings, Ishibashi and Shimomura, individually or in combination, fail to overcome the deficiencies of Jin. Therefore, the combination of Jin, Ishibashi and Shimomura, fails to render the limitations of independent claim 1 obvious to one of ordinary skill in the art.

Applicant, therefore, respectfully requests that the rejection to claim 1 under 35 U.S.C. § 103 be withdrawn.

With regards to claims 2-8, Applicant respectfully asserts that claims 2-8 are dependent upon claim 1 and claim 1 has been shown patentable at least for the reasons set forth above. Therefore, claims 2-8 are patentable at least by reason of their dependency. For at least this reason, Applicant respectfully requests that the rejections of claims 2-8 be withdrawn.

## CONCLUSION

In view of the above remarks, Applicants respectfully submit that each of the rejections has been addressed and overcome, placing the present application in condition for allowance. A notice to that effect is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to contact the undersigned.

Pursuant to 37 C.F.R. §1.17 and 1.136(a), Applicant hereby petitions for a one (1) month extension of time for filing a reply to the outstanding Office Action and submits the required $130.00 extension fee herewith.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Donald J. Daley, Reg. No. 34,313 at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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By _____

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